

Lithographically Patterned Nanowire Electrodeposition: A Method for Patterning Electrically Continuous Metal Nanowires on Dielectrics

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The fundamental optical and electrical properties of metal nanowires are increasingly of interest to scientists. Until very recently,^{1–3} investigations of the electrical properties of metal nanowires have concentrated on relatively short wires ($l < 10 \mu\text{m}$)^{4,5} prepared using electron beam lithography (EBL)⁶—a technique in which wires as narrow as 20 nm can be prepared by exposing a polymer resist using a focused electron beam. A “direct write” method⁷ for preparing 30 nm diameter palladium nanowires using a focused electron beam in conjunction with organometallic precursor has very recently been described.⁸ Long ($>100 \mu\text{m}$) nanowires are desirable for the elucidation of the optical properties of metal wires,^{9–11} and there is increasing activity focused on optical investigations of periodic arrays of metal meshes^{12–14} and nanowires^{15–17} that cannot readily be fabricated using the slow, serial EBL technology. Motivated by these considerations, many new methods for preparing metal nanowires have been described and we discuss some of these below.

Single crystalline metal nanowires can be prepared using solution phase methods developed by the research groups of El-Sayed,^{18,19} Murphy,^{20–22} Xia,^{23–25} and others. With continued refinement, the maximum length of the metal nanowires that can be prepared using these approaches continues to grow and in the case of silver, for example, the maximum lengths are now in the 50 μm range.²⁵ However, such nanowires are typically isolated as orientationally random powders and the

ABSTRACT Lithographically patterned nanowire electrodeposition (LPNE) is a new method for fabricating polycrystalline metal nanowires using electrodeposition. In LPNE, a sacrificial metal ($M_1 = \text{silver or nickel}$) layer, 5–100 nm in thickness, is first vapor deposited onto a glass, oxidized silicon, or Kapton polymer film. A (+) photoresist (PR) layer is then deposited, photopatterned, and the exposed Ag or Ni is removed by wet etching. The etching duration is adjusted to produce an undercut $\approx 300 \text{ nm}$ in width at the edges of the exposed PR. This undercut produces a horizontal trench with a precisely defined height equal to the thickness of the M_1 layer. Within this trench, a nanowire of metal M_2 is electrodeposited ($M_2 = \text{gold, platinum, palladium, or bismuth}$). Finally the PR layer and M_1 layer are removed. The nanowire height and width can be independently controlled down to minimum dimensions of 5 nm (h) and 11 nm (w), for example, in the case of platinum. These nanowires can be 1 cm in total length. We measure the temperature-dependent resistance of 100 μm sections of Au and Pd wires in order to estimate an electrical grain size for comparison with measurements by X-ray diffraction and transmission electron microscopy. Nanowire arrays can be postpatterned to produce two-dimensional arrays of nanorods. Nanowire patterns can also be overlaid one on top of another by repeating the LPNE process twice in succession to produce, for example, arrays of low-impedance, nanowire–nanowire junctions.

KEYWORDS: nanowire · photolithography · electrodeposition · noble metal

incorporation of individual nanowires into electrical circuits or optical devices poses a significant challenge.²⁶

Template synthesis (for reviews, see refs 27–29) provides a popular and highly versatile means for synthesizing polycrystalline metal nanowires within the nanoscopic cylindrical pores of an alumina or polymer membrane material but most applications for these nanowires require their release from these templates producing, once again, an orientationally disordered powder with its attendant challenges for device fabrication.

A variety of other innovative nonlithographic methods for preparing ultralong polycrystalline metal nanowires have been demonstrated. An advantage of all these methods is that the metal nanowire is

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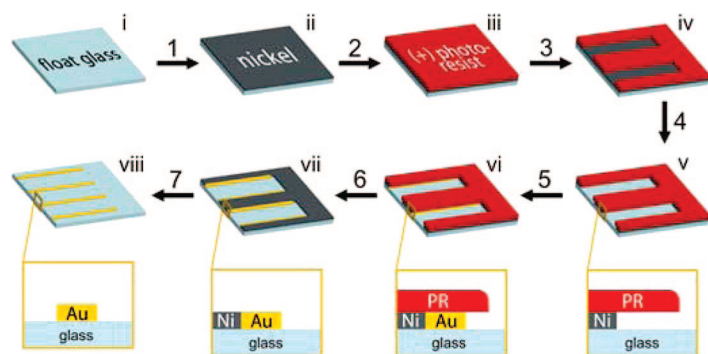


Figure 1. Process flow for the formation of gold nanowires using the seven-step LPNE method.

produced on a surface with some degree of control over its orientation. Jorritsma *et al.*^{30,31} used anisotropic etching to produce two-dimensional grooves on InP surfaces. The protruding InP “teeth” were then decorated with tantalum by evaporative deposition at grazing incidence to produce 20 nm width nanowires. Using the layer thickness precision afforded by molecular beam epitaxy, Natelson and co-workers^{32,33} created a single GaAs–AlGaAs–GaAs quantum well. Fracturing this layered structure exposed the layer in cross-section and preferential etching of the AlGaAs layer then produced a trench with nanometer-scale width and depth. This trench was used to template a platinum nanowire prepared by evaporative deposition. Nanowires as small as 3 nm in width were formed using this approach. Heath and co-workers parallelized this process using multiple AlGaAs quantum well structures, to produce arrays of nanowires composed of silicon,³⁴ platinum,³⁵ and bismuth.³⁶ Whitesides and co-workers^{37,38} embedded a metal film with nanometer-scale thickness in an epoxy matrix and sectioned it using an ultramicrotome to produce nanowires that are embedded within an epoxy sheet that can be positioned on a dielectric. Removal of the epoxy using an oxygen plasma produces wires or aligned, colinear wire arrays, and other nanowire topologies. Laser interference lithography was employed by Nielsch and co-workers³⁹ to prepare a defect pattern that promoted the nucleation of metal and the formation of metal nanowires by electrodeposition. Patterned copper nanowires as small as 40 nm were obtained using this approach. Buriak and co-workers^{40–42} used block copolymers as templates to form electrically continuous platinum nanowires. Electrochemical step edge decoration (ESD)^{43–45} is a related method in which the quasi-linear step edge defects present on graphite surfaces are exploited to nucleate metal nanowires by electrodeposition. Antimony nanowires as small as 35 nm have been prepared using this approach.⁴⁶ But, none of these methods provide the flexibility to position nanowires in arbitrary patterns on a surface in order to enable a function for these wires as interconnects, circuit elements, optical transducers, *etc.*

One potential solution to the “nanowire patterning problem” is to conformally coat photolithographic masks with a uniform layer of material to make them smaller. In 2001, Weiss and co-workers⁴⁷ demonstrated a version of this strategy in which a lithographic mask was derived from a patterned gold layer coated with a self-assembled layer of *n*-alkylthiol molecules. The line-widths of metal wires formed using these metal–organic hybrid resists were as small as 15 nm. Using a similar strategy, Steinhogel and co-workers scaled down the dimensions of microfabricated trenches in an a-silicon mask by chemical vapor deposition of a conformal layer of Si₃N₄. The Damascene method was then used to fill these trenches with copper^{2,48} and tungsten³ nanowires.

We have recently described⁴⁹ a new method for patterning electrodeposited noble metal nanowires on glass using photolithography. This method, called Lithographically patterned nanowire electrodeposition (LPNE), involves the fabrication by photolithography of a temporary, sacrificial template on the glass surface composed of photoresist and a metal film. We have already demonstrated⁴⁹ that LPNE provides the means for patterning noble metal nanowires with lateral dimensions down to 18 nm (w) × 40 nm (h) on glass surfaces. These nanowires can be 1 cm or more in total length. In this full paper, we explore the capabilities of LPNE to produce nanowires of gold, platinum, palladium, and the base metalloid, bismuth, on glass, oxidized silicon, and flexible Kapton films. We also describe variations on the LPNE method that enable the fabrication of potentially useful nanowire architectures including crossed nanowire networks and nanorod arrays. Finally, the in-depth electrical and structural characterization of these nanowires is reported for the first time. An issue on which we focus particular attention is the grain structure of these nanowires because the reflection of conduction electrons at grain boundaries is one of two dissipation mechanisms responsible for electrical resistance in these materials. In fact, we will conclude that grain boundaries make a far larger contribution to the resistance of gold and palladium nanowires than the diffuse scattering of electrons from wire surfaces.

RESULTS AND DISCUSSION

Metal Nanowire Fabrication using LPNE. The seven-step process flow for the LPNE method (Figure 1) was identical for gold, platinum, and palladium metals deposited here except for the metal plating electrochemistry in step 5. For bismuth, an evaporated silver layer was substituted for nickel. Briefly, the LPNE process involved the thermal evaporation of the nickel or silver film onto a glass, oxidized silicon, or Kapton surface (step 1). The thickness of this film determined the ultimate thickness of the nanowires produced using this method. Then a (+) photoresist (PR) layer was deposited by spin-

TABLE 1. Average Grain Size of Gold, Palladium, Platinum, and Bismuth Nanowires

metal	experimental method		
	GIXRD ^a (nm)	TEM ^b (nm)	electrical ^c (nm)
Au	14.0	39 ± 11	70.8 ± 0.3
Pd	15.3	20 ± 7	22 ± 2
Pt	7.9	4.91 ± 1.21	
Bi	25.5	3.86 ± 0.29	

^aGIXRD = grazing incidence X-ray diffraction. ^bTEM = transmission electron microscopy. ^cCalculated from the best fit of eqs 2 and 3 to the temperature-dependent nanowire resistance.

coating, it was soft-baked at 90 °C for 30 min (step 2), and a contact mask was used to pattern this PR using 365 nm illumination (step 3). After developing this pattern, the exposed nickel was removed by etching in 0.80 M nitric acid, and exposed silver was removed using 18% NH₄OH and 4% H₂O₂ (step 4). The duration of etching was adjusted to produce an ≈300 nm undercut along the perimeter of the photoresist, and it varied somewhat depending on the thickness, *t*, of the metal film. Now, this surface was immersed in a dilute metal plating solution in which the concentration of metal was between 0.2 and 6 mM and metal was potentiostatically electrodeposited for between 5 and 500 s depending on the metal and the width of the nanowire that is targeted (step 5). Then, the PR layer was removed by washing with acetone (step 6), and the patterned nickel or silver layer was removed using a second etch in the same solution as used in step 4 (step 7).

The procedure for removing the metal layer in step 5 departs from the procedure we published earlier⁴⁹ in which the nickel layer was removed by electrooxidation. We now use solution-phase etching for both silver and nickel for a reason that is apparent when the trench formed by etching is viewed in cross-section using scanning electron microscopy (SEM; Figure 2). Electrochemical etching produces a metal edge profile that is angled at 60° relative to vertical (Figure 2a). We were unable to improve upon this profile by adjusting the etch rate using either the etching potential or the composition of the electrolyte. If this metal edge is employed for nanowire growth, a wedge-shaped nanowire is produced. If instead the metal layer is removed using a solution-phase etchant, a nearly vertical nickel edge profile is obtained (Figure 2b). The resulting trench, and the nanowire obtained from it, has a precisely defined height that matches the metal layer thickness, as demonstrated below.

Nickel was employed as the sacrificial electrode material (Figure 1) because it can be selectively removed in step 7 using nitric acid without damaging nanowires composed of gold, palladium, or platinum. From an electrochemical perspective, however, nickel is a challenging electrode material because it is susceptible to oxidation—particularly in the basic electrolyte used for the deposition of gold.⁵⁰ Cyclic voltammograms ac-

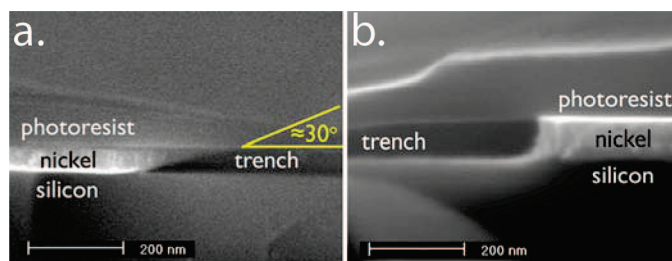


Figure 2. Cross-sectional images of two horizontal trenches showing the profile of the nickel edge prepared by (a) electrochemical etching and (b) wet etching with 0.8 M HNO₃.

quired in the metal plating solutions used in this study (Figure 3) clearly manifest this problem. For Au, Pd, and Pt, the first voltammetric scan from positive to negative potentials produces a smaller cathodic deposition current than the reverse, positive-going scan (Figure 3a–c) in defiance of convention.⁵¹ This “activation” of the metal deposition reaction occurs because of the progressive replacement of the nickel edge with a noble metal edge as the noble metal is deposited; the deposition reaction at the noble metal edge is kinetically faster than at nickel. The silver edge employed for bismuth deposition, on the other hand, is not activated by the deposition of bismuth (Figure 3d) because bismuth is a much poorer electrode material than silver with a greater susceptibility to oxidation and higher electrical resistivity (Table 1).

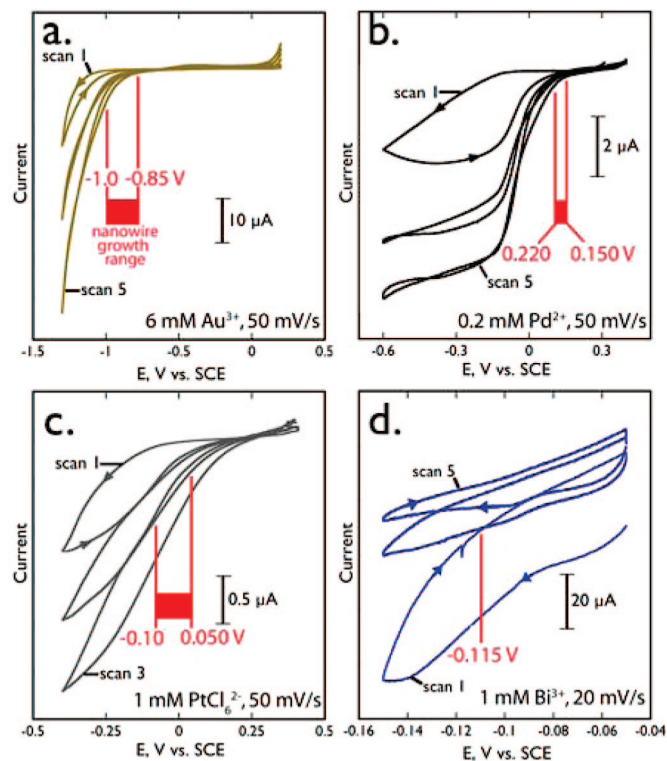


Figure 3. Cyclic voltammograms (scan rates as indicated) acquired in the metal plating solutions employed for nanowire growth: (a) gold, (b) palladium, (c) platinum, (d) bismuth. The range of electrodeposition potentials employed for potentiostatic electrodeposition of nanowires are indicated in red.

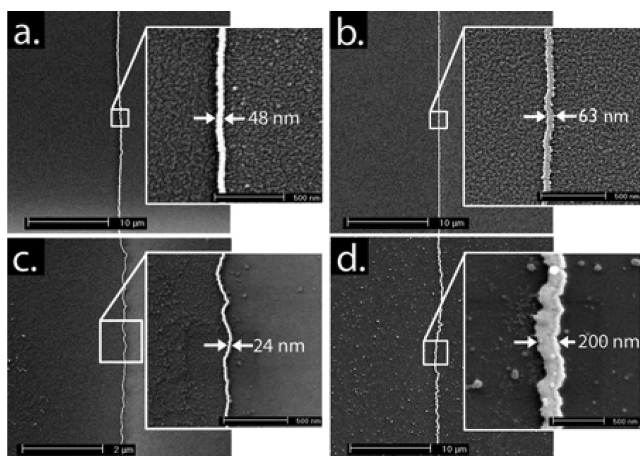


Figure 4. Scanning electron micrographs of linear nanowires: (a) gold, (b) palladium, (c) platinum, (d) bismuth.

The result, seen in Figure 3d, is that the bismuth deposition rate is highest for the first, negative-going scan, and progressively slower on each successive scan. In spite of the disparate voltammetric behavior observed for these four metals at the patterned metal edge (Figure 3), nanowires were routinely obtained for all four metals by potentiostatic deposition from these plating solutions. The range of potentials that can be used to obtain nanowires is indicated for each metal in red in Figure 3. The insensitivity of the LPNE process to the detailed electrochemistry of the metal plating solution is one of its attributes.

Structural Characterization. The LPNE method produces nanowires with a rectangular cross-section and a flat

top. Scanning electron micrographs of linear nanowires of Au, Pd, Pt, and Bi on glass are shown at both low and high magnification in Figure 4. The low magnification images clearly show that the path of these nanowires on the glass is not perfectly linear, and some “wandering” of the nanowire trajectory about a straight path on the surface is seen—especially in Figure 4c and d. All of these nanowires were produced in an unfiltered laboratory air ambient, and we have verified that the imprecision seen in the nanowire position on the surface reflects the influence of contamination on the photolithography implicit in the LPNE process. In spite of this positioning imprecision, the wire width is narrowly distributed about a mean value that is different for each of the nanowires shown here. This wire width can be systematically varied from a minimum value of 11–30 nm to hundreds of nanometers, depending on the metal and the electrodeposition parameters including the deposition time, solution composition, and the applied potential as shown in Figure 5b.

The wire height is dictated by the thickness of the metal layer deposited in the first step of the LPNE process (Figure 5a). Cross-sectional profiles for typical gold nanowires, measured by AFM, show the vertical wire edges and the flat top surface produced by the LPNE method (Figure 5c). Minimum values for the wire height are in the 5–8 nm range for all four metals. Importantly, the wire width and height can be reliably adjusted over the full ranges shown in Figure 5a and b without cross-talk between these two parameters. How uniform are the width and height dimensions of these

nanowires? Standard deviations of the measured wire width and height are plotted as the error bars in Figure 5a and b. The relative standard deviation, RSD_w , for the width dimension is lowest for gold ($RSD_{w,Au} = 15\%$, averaged over all samples) and highest for platinum ($RSD_{w,Pt} = 28\%$) with bismuth and palladium intermediate between these two limits. For all metals, this RSD_w shows a weak inverse correlation with the width magnitude, so it is $\approx 5\%$ higher than this mean value for the smallest wires. The height dimension is better controlled for all four metals, with RSD_h in the range from $RSD_{h,Bi} = 6\%$ to $RSD_{h,Pd} = 14\%$.

Patterns of gold nanowires produced by LPNE are shown in Figure 6. The spiral pattern shown in Figure 6a and b produces a nanowire with a total contour length of ≈ 2.7 cm. Arrays of thousands of linear nanowires, each a centimeter in length and deposited at $2 \mu\text{m}$ pitch (Figure 7a) can be used to carry out powder X-ray diffraction measurements using grazing incidence X-ray diffraction

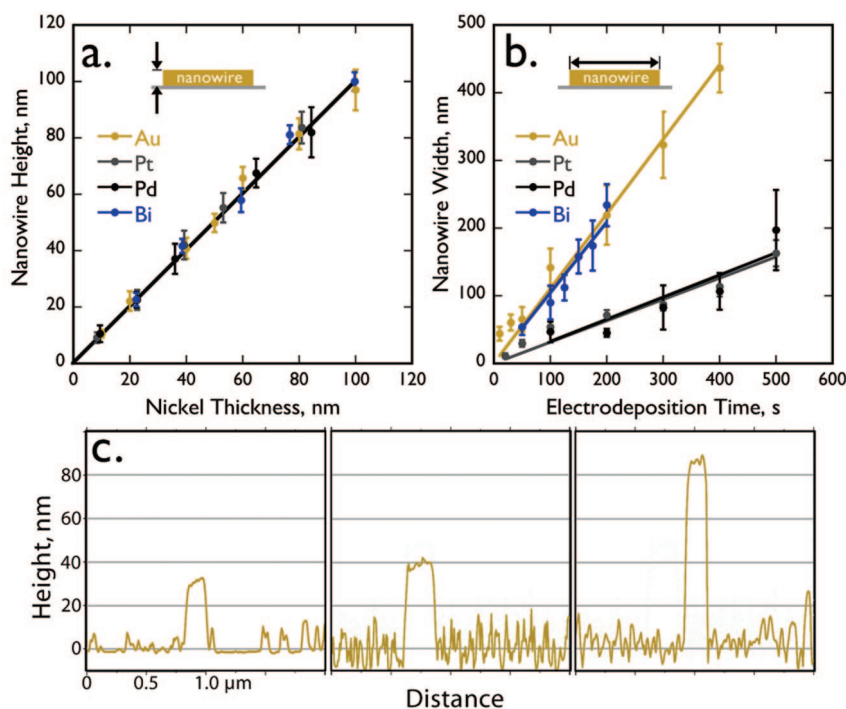


Figure 5. Control of nanowire height and width for wires of Au, Pt, Pd, and Bi. (a) Nanowire height measured by AFM versus the thickness of the nickel or silver sacrificial layer. (b) Nanowire width measured by SEM versus the electrodeposition duration. (c) Nanowire cross-sectional profiles measured by atomic force microscopy.

(GIXRD, Figure 7b). Typical GIXRD patterns for all 4 metals (Figure 7c) show 4–5 assignable reflections for fcc Au, Pd, and Pt and more than 12 reflections for the rhombohedral unit cell of bismuth. In all cases, these patterns were acquired for nanowires deposited on glass and a broad envelope centered at 25° is contributed by diffraction from the glass surface. If the contribution of lattice strain to the X-ray line-width is negligible the Debye–Scherrer equation can be used to estimate the grain diameter, d :⁵²

$$d = \frac{0.9\lambda}{B \cos \theta_B} \quad (1)$$

where λ is the X-ray wavelength, B is the line width, and θ_B is the scattering angle. A real-space measurement of the in-plane value of d can be derived from transmission electron micrographs (Figure 8). Together, GIXRD and TEM afford an estimate of the grain dimension both in the plane of the surface (TEM) and perpendicular to it (GIXRD). It is important to recognize, however, that GIXRD measures d over a range of angles (relative to the surface normal) from 5° ($2\theta = 10^\circ$) to 45° ($2\theta = 90^\circ$). This means that, for the most intense, low-angle GIXRD lines, the measurement of d is bounded by the wire thickness (40 nm for all four metals) and the measured value for d will be meaningful only when the grain diameter is smaller than this limit.⁵³ A comparison of the experimentally measured values for d from these three methods are compared in Table 1.

Electrical Characterization. Electrically continuous metal nanowires that are millimeters in total length can be prepared using the LPNE method. A survey of 45 nm (h) \times 302 nm (w) by 5 mm (l) gold nanowires deposited in a linear array showed that 70% of these wires were electrically continuous over their entire length. In these ultralong nanowires, breaks are most often caused by the corruption of the lithography process by dust particles.

The temperature-dependent resistance of single gold, palladium, and bismuth nanowires were measured from 300 to 20 K using an evaporated gold four-point probe (Figure 9a) that isolated 100 μm sections of each nanowire. For all three metals, current–voltage plots were ohmic over the entire temperature range, as shown for gold in Figure 9b, and the slope of

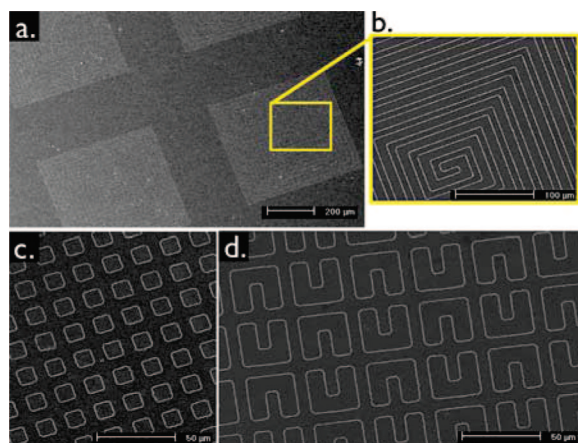


Figure 6. Gold nanowires fabricated by LPNE. (a and b) Coiled nanowires with a total contour length of ≈ 2.7 cm. (c) Nanowire loops. (d) U-shaped nanowires.

these I–V plots were used to calculate the resistance of each wire, R , at each temperature point. The resistivity of the nanowire, ρ , was calculated from: $\rho = AR/L$ where A is the cross-sectional area of the nanowire and L is the electrically isolated length.

Previously, bismuth nanowires have been intensively studied^{54–59} because of the unique and strongly size-dependent electronic properties of bismuth, an indirect semimetal, conferred by its band structure.^{56,57} In particular, bismuth nanowires are predicted to exhibit a semimetal-to-semiconductor transition at a critical lateral dimension of ≈ 50 nm.³⁶ Bismuth also has an extremely long mean free path of ≈ 1 mm for single crystals, and boundary scattering causes an increase of the resistance above the bulk value for films or wires with a smallest dimension below this. Just one previous paper reports four-contact resistivity measurements on

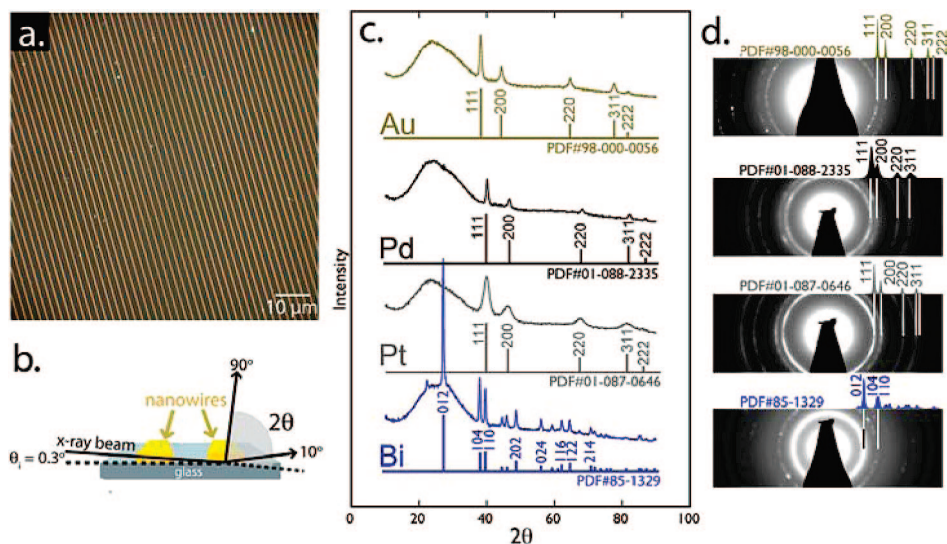


Figure 7. Crystallographic structural characterization of four different metals. (a) Optical micrograph of linear nanowires deposited at 2 μm pitch used for the acquisition of GIXRD data. (b) Schematic diagram of GIXRD for nanowire arrays on glass substrate. (c) X-ray diffraction patterns obtained from metal nanowire arrays prepared by LPNE. For each metal, the predicted pattern is shown below the experimental data, together with the assignment of each reflection. (d) Selected-area electron diffraction (SAED) patterns and assignments for metal nanowires.

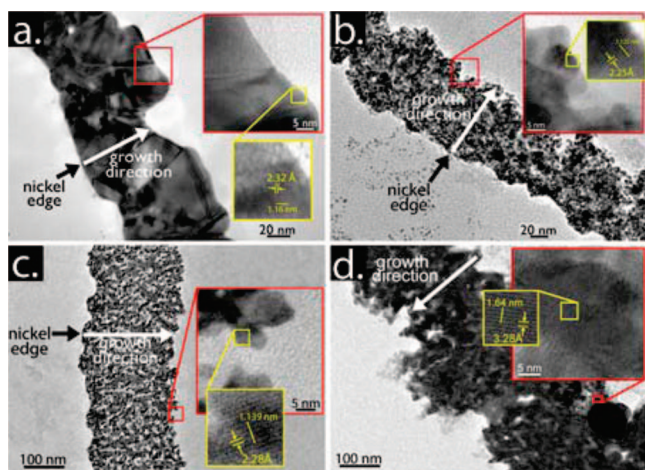


Figure 8. Transmission electron micrographs of four different metals with high resolution lattice fringes (inset). (a) Gold. (b) Palladium. (c) Platinum. (d) Bismuth. Nanowire growth directions are indicated by arrows.

bismuth nanowires,³⁶ analogous to the measurements we report here, and in that work, the electrically isolated wire length was $\approx 2 \mu\text{m}$. We measured $100 \mu\text{m}$ lengths of two relatively large nanowires with dimensions of $260 \times 652 \text{ nm}$ and $96 \times 289 \text{ nm}$, and both of these wires showed an increased resistance with decreasing temperature (Figure 8c; Table 2), characteristic of semiconducting materials and qualitatively as observed previously for bismuth nanowires in this size regime.^{54–59} Measured resistances for the larger of these two nano-

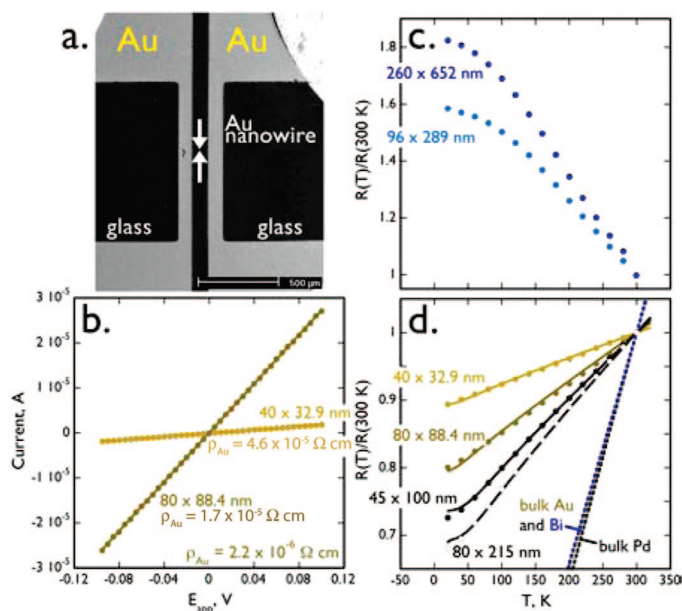


Figure 9. Electrical characterization of single gold, palladium, and bismuth nanowires. (a) Scanning electron micrograph of a single gold nanowire with four-point gold electrodes (thickness = 60 nm) evaporated through a shadow mask. This mask isolated a $100 \mu\text{m}$ length of a single metal nanowire. (b) Current-versus-voltage curves of gold nanowires with two different dimensions, as indicated. (c) Temperature dependence of the bismuth nanowire resistance, R , normalized to the resistance at 300 K , $R_{300\text{K}}$, from 20 to 300 K . (d) Temperature dependence of the gold and palladium nanowire resistance, R , normalized to the resistance at 300 K , $R_{300\text{K}}$, from 20 to 300 K .

wires ($\rho_{300\text{K}} = 359 \Omega \text{ cm}$ and $\rho_{20\text{K}} = 654 \Omega \text{ cm}$) were in the range reported previously for wires in this size regime (Table 2) while the resistances seen for the smaller wire were higher by approximately 50% , perhaps as a consequence of the smaller grain diameter of our materials (Table 1). Quantitative theoretical predictions of the wire resistivity have not been possible for bismuth because of its complexity.⁵⁷

A more quantitative comparison of the measured temperature-dependent resistance with theory is possible with metal nanowires but there is very little data on either gold or palladium in the literature. The electrical resistivity of copper^{2,48,60,61} and tungsten³ nanowires with a rectangular cross-section has been reported by Steinhogel and co-workers. These workers derived an equation^{2,61} that related the measured wire resistivity, ρ , to its height and width, the temperature-dependent bulk resistivity of the metal, ρ_0 , and three additional parameters: the grain diameter, d , the specularly parameter, p , which is the fraction of surface scattering events that preserve momentum, from Fuchs-Sondheimer theory,^{62,63} and R , the “reflectivity coefficient”, the fraction of electrons that are scattered by the potential barrier presented by grain boundaries, from Mayadas–Shatzkes theory.⁶⁴

$$\rho = \rho_0 \left\{ \frac{1}{3} \left[\frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 \ln \left(1 + \frac{1}{\alpha} \right) \right] + \frac{3}{8} C (1-p) \frac{1+AR}{AR} \frac{\lambda}{w} \right\} \quad (2)$$

with

$$\alpha = \frac{\lambda}{d} \frac{R}{1-R}$$

Other parameters in eq 2 are the following: w , the nanowire width, AR , its aspect ratio ($AR = \text{height}/\text{width}$) C , a geometrical parameter, which is equal to 1.2 for nanowires with a rectangular cross-section, and λ , the electron mean free path. The accuracy of eq 2 is 3.5% for nanowires with dimensions down to 50 nm .^{2,61} In eq 2, the temperature dependent ρ_0 is calculated using the Block–Grüneisen equation:⁶⁵

$$\rho_0(T) = C \frac{T^5}{\theta^6} \int_0^{\theta/T} \frac{x^5}{(e^x - 1)(1 - e^{-x})} dx \quad (3)$$

where θ is the Debye temperature of the metal ($\theta_{\text{Au}} = 165 \text{ K}$, $\theta_{\text{Pd}} = 274 \text{ K}$) and C is a constant that depends on the metal ($C_{\text{Au}} = 9.0 \times 10^{-6} \Omega \text{ m}^{-1} \text{ K}$, $C_{\text{Pd}} = 1.1 \times 10^{-4} \Omega \text{ m}^{-1} \text{ K}$).

Equations 2 and 3 were used to model the temperature-dependent resistances of single gold and palladium nanowires using p , R , and d as fitting parameters (Table 2). The first conclusion of interest is that, for both gold and palladium, the contribution of grain

TABLE 2. Summary of Measured Electrical Properties for Gold, Palladium, and Bismuth Nanowires and Comparison with Literature Values

metal	h × w (nm)	ρ_{300K} ($10^{-5} \Omega \text{ cm}$)	ρ_{20K} ($10^{-5} \Omega \text{ cm}$)	p^a	R^b	d^c (nm)
Au	40 × 33	4.63	4.14	0.374	0.895	70.4
	80 × 88	1.71	1.37	0.384	0.8	71.1
	bulk ⁶⁷	0.227	0.0035			
Pd	45 × 100	35.2	25.6	0.227	0.794	18.8
	80 × 215	21.3	14.5	0.238	0.806	24.7
	bulk ⁶⁷	1.08	0.00563			
Bi	96 × 289	1056.1	1673.7			
	261 × 652	359	654.3			
	bulk ⁶⁷	10.7				
literature						
Au ⁴	20 × 60	0.68		0.5	0.9	
Pt ⁶⁸	70 in diameter	3.3		0.177	0.227	
Bi ⁶⁹	50 × 70; 50 × 120; 50 × 200	405; 287; 230			0.5	
Bi ³⁶	25 × 72; 15 × 55; 15 × 28	130; 95; 550; 660				

^aThe specularity of electron scattering at wire surfaces. ^bThe reflection coefficient for electrons at grain boundaries. ^cAverage grain diameter.

boundary scattering to the total resistance is at least a factor of 10 greater than the contribution of surface scattering; qualitatively in agreement with the observations of both Steinhogel *et al.*⁶¹ and Durkan and Welland.⁴ The value of R derived from the fits of Eqs 1 and 2 are in the range from 0.8 to 0.9 for all four wires of both metals and this is consistent with the estimate for gold nanowires⁴ of $R \approx 0.9$. The value of p obtained from this fit was smaller for palladium ($p \approx 0.23$) than for gold ($p \approx 0.38$) by approximately 30% (Table 2). The only literature measurement of p for gold nanowires⁴ yielded a value of 0.5. For palladium nanowires, the grain size derived from this resistivity analysis of 22 nm matches the grain size estimated using TEM and GIXRD within experimental error (Table 1). For gold, this “electrical” d is 71 nm which is somewhat larger than the d estimated from TEM (39 nm) and GIXRD (14 nm) but of the same order of magnitude. This analysis leads to the conclusion that the electrical behavior of long palladium and gold nanowires prepared by LPNE approximates the expected behavior for these nanowires based upon their known lateral dimensions and grain size.

Variations on the LPNE Method. There is interest in preparing nanowires on flexible substrates for a variety of applications.⁶⁶ Heath and co-workers⁶⁶ transferred silicon nanowires deposited on silicon surfaces to flexible polydimethylsiloxane (PDMS) surfaces. The LPNE process can be used to directly deposit long (>1 mm) gold and bismuth nanowires on flexible Kapton films (Figure

10). The procedure for Kapton substrates is identical to that for glass or oxidized silicon (Figure 1), and 100 μm segments of these nanowires have an electrical resistivity that is approximately equal to the measured values seen for comparable nanowires on rigid surfaces.

The nanowire length dimension, as well as its width and height, can be modified by removing nanowire segments after LPNE deposition. This is accomplished by adding a second lithographical patterning step to the baseline 7 step LPNE process: Onto the already fabricated metal nanowires, a photoresist layer is deposited and photopatterned to expose sections of the metal wires that are then removed by a chemical etching step. In the case of gold nanowires; for example, we employed a iodide/triiodide etching solution (16 mM KI_3 and 8 mM KI). Gold nanorod arrays (Figure 11) can be produced from linear nanowire arrays using this approach.

The postprocessing of LPNE nanowires can be taken one step further by repeating the entire process twice in succession. This enables nanowire patterns to be overlaid one on top of another. In the simplest example of this process, an array of crossed nanowire junctions is obtained by depositing two

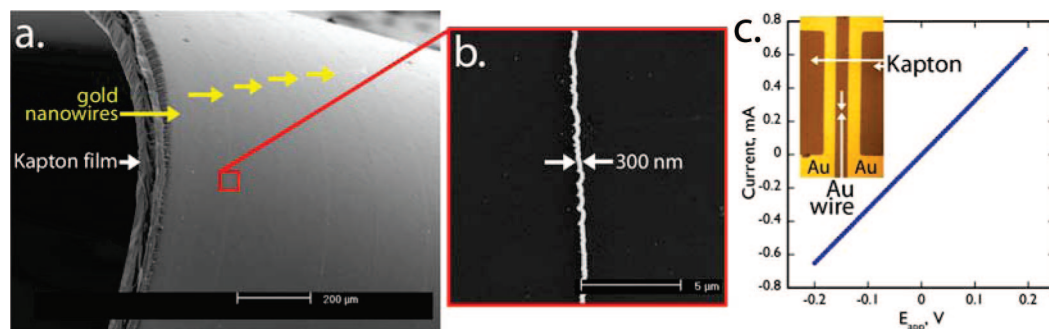


Figure 10. Gold nanowires on a flexible Kapton film: (a and b) Low and high magnification scanning electron micrographs of gold nanowires on a Kapton film. (c) Current-versus-voltage curves acquired using four-point evaporated electrical contacts (insert).

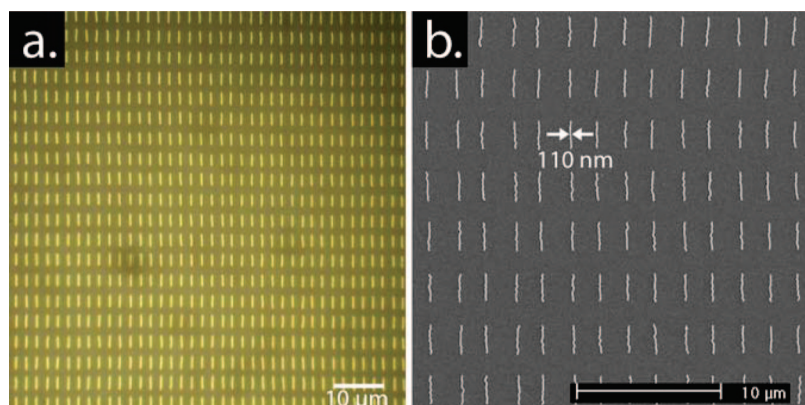


Figure 11. Gold nanorods prepared by masking ultralong gold nanowires with a lithographically patterned photoresist and then etching to remove exposed wire segments. (a) Optical micrograph of gold nanorods with 2 μm spacing. (b) High magnification SEM image of gold nanorods with dimensions of 110 nm \times 40 nm \times 2 μm .

sets of parallel nanowires oriented at 90° with respect to one another (Figure 12a and b). Electrically continuous wire–wire junctions are obtained by this dual LPNE process. The electrical characterization of one such junction (Figure 12c) involves the measurement of current *versus* voltage curves for three wires emerging from a crossed junction against the fourth. The electrically isolated lengths of these four wire segments were similar ($\approx 100 \mu\text{m}$) so the similarity of I – V traces 1 and 3, in which the interwire junction is crossed, with trace 2, in which the interwire junction is not crossed, suggests that the electrical

broadly consistent with the known lateral dimensions and grain diameters of these wires. Uniquely, LPNE is capable of patterning a square centimeter with a grid of linear metal nanowires patterned at a 2 μm pitch within 5–6 h—a task that would require ≈ 500 h for the exposure step alone using electron beam lithography with a typical write-speed of 10 cm h^{-1} .

In this work, we have concentrated attention on gold, palladium, platinum, and bismuth but nanowires composed of other metals will be accessible using this approach. The main issue in this regard is the stability of the metal nanowire in the presence of the solution employed for removal of that layer in step 7 of the process. In addition to nickel and silver, we have successfully employed gold layers—removable using an acidic iodide/triiodide etch.

Grain diameters in the nanowires examined here ranged from ≈ 15 –39 nm for gold to ≈ 5 –8 nm for platinum. A challenge going forward is the development of methods for growing the grain size of these nanowires either using the electrodeposition conditions or *via* thermal postprocessing while retaining control over the shape and lateral dimensions of these structures.

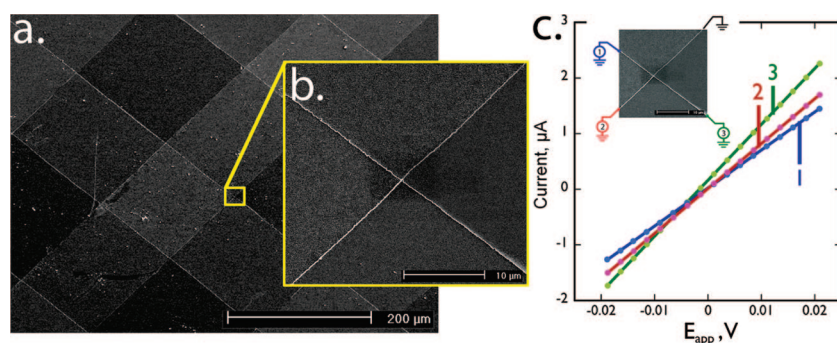


Figure 12. Crossed gold nanowires prepared by carrying out the LPNE twice in succession (but with rotation of the mask by 90°). (a and b) Low and high magnification SEM images of crossed gold nanowires on glass. (c) Current-*versus*-voltage curves for a typical nanowire-nanowire junction showing I – V curves acquired at three nanowire ends relative to a common ground wire.

METHODS

Nanowire Fabrication. The 7-step LPNE procedure shown in Figure 1 was implemented as follows: Soda lime glass microscope slides were cleaned in aqueous Nochromix solution, air-dried, and diced into 1 in. \times 1 in. squares. For wire growth on flexible substrates, Kapton 100HN films were cleaned in acetone and pure water and then cut into 1 in. \times 1 in. squares. Oxidized silicon wafers (p-type, (100)-oriented) were used for low temperature electrical measurements. These were degreased with methylene chloride and diced into 1 in. \times 1 in. squares. When using silver as the sacrificial electrode, glass or silicon substrates were

exposed for 8–12 h to a toluene solution of 0.2% APTES (Sigma-Aldrich), to promote the adhesion of the silver layer to the substrate. This treatment was not necessary for depositions onto Kapton films. Onto each square of soda lime glass, silicon, or Kapton, a nickel or silver film (ESPI, 5N purity) 10–200 nm in thickness was deposited by physical vapor deposition (PVD) at a rate of 0.5–1.5 \AA s^{-1} (step 1). The film thickness and evaporation rate were monitored using a quartz crystal microbalance (Sigma Instruments). A positive photoresist (PR) layer of Shipley 1808 was then deposited onto these nickel-coated surfaces by spin coating (1 mL aliquot, 2500 rpm for 80 s). This PR layer was then soft-

resistance of the junction is much smaller than the series resistance of any two of these $\approx 100 \mu\text{m}$ wire segments.

CONCLUSIONS

The LPNE method is a new and versatile tool for fabricating metal nanowires in a highly parallel fashion directly on dielectrics ranging from glass to flexible plastic. These nanowires have a rectangular cross-section with height and width dimensions that can be independently specified in the range from 11 nm to 2 μm (w) and 5–200 nm (h). Long, 100 μm segments of these wires are electrically continuous and, in the case of gold and palladium, these nanowires show a temperature-dependent resistivity that is

baked at 90 °C for 30 min to produce a PR layer thickness of \approx 500 nm. After cooling to room temperature, the PR was patterned using a contact mask in conjunction with a commercial mask alignment fixture (model 83210 Newport Corporation), a UV light source (i-line, 365 nm \times 1.5 s, model 97434 Newport Corporation) and a digital exposure controller (model 68945 Newport Corporation). The exposed PR layer was developed in Shipley MF-319 for 20 s, rinsed in water, and dried in a stream of ultrahigh purity (UHP) N₂ (step 3). Exposed nickel was then removed by etching with 0.8 M nitric acid solution for 2–10 min depending on the thickness of the nickel film (step 4). In the case of silver films, etching involved exposure to a solution of 18% ammonium hydroxide (Fisher ACS) and 4% hydrogen peroxide (Fisher ACS 3%) for 30 min. This process, described in greater detail below, also produced a horizontal trench delineated on three sides by the PR layer, the nickel or silver edge, and the glass or Kapton surface at the periphery of the exposed region.

Into this trench, palladium, platinum, gold, or bismuth were electrodeposited (step 5) using the recessed nickel (Au, Pd, Pt) or silver (Bi) edge located within it. The electrodeposition of these four metals was carried out in a 50 mL, one compartment, three-electrode cell. Palladium was electroplated from a solution containing 0.1 M KCl, 0.22 M EDTA, and 0.2 mM PdCl₂ at 0.20 V vs a saturated calomel reference electrode (SCE). Platinum was electroplated from a solution containing 0.1 M KCl, and 1.0 mM K₂PtCl₆ at 0.025 V vs SCE. Gold was electroplated from an aqueous commercial gold plating solution (Clean Earth Solutions, Carlstadt, NJ) that was 6 mM in AuCl₃ solution, pH = 9.78) at -0.90 V vs SCE. Bismuth was electroplated from a solution containing 1 mM Bi(NO₃)₃ · 5(H₂O) and the following additives: boric acid (20 mM), tartaric acid (20 mM), NaCl (20 mM), K₂SO₄ (10 mM), Bi(NO₃)₃ · 5H₂O (1 mM), glycerol (3 mM), HNO₃ (0.07 M), and gelatin (1.2%). The plating potential for bismuth was -0.115 mV vs SCE. All aqueous solutions were prepared using Millipore MilliQ water ($\rho > 18.0$ M Ω cm). A saturated calomel reference electrode (SCE) and a 2 cm² Pt foil counter electrode were also employed. The metal deposition was carried out on a computer-controlled Gamry Instruments G300 Series potentiostat/galvanostat. After the deposition of the nanowire in step 5, the photoresist was removed (step 6) by rinsing the slide with electronic grade acetone (Acros) and Millipore water before drying with UHP N₂. The excess nickel film was then removed by washing with dilute HNO₃ (step 7).

X-ray Diffraction. X-ray diffraction patterns for electrodeposited nanowires were acquired on the surface on which they were electrodeposited by utilizing low angle incidence X-ray diffraction (LIXRD),^{70–72} in which the incident angle is below the critical angle. In this limit, X-rays are totally externally reflected by the sample limiting the penetration into the sample surface to a few nanometers thereby improving the signal-to-background ratio for reflections involving nanostructures located on top of the sample surface. Arrays of linear nanowires deposited at 2 μ m pitch over a 1 cm \times 1 cm area were employed for this purpose. LIXRD was performed using parallel beam optics and an incident angle of 0.3° on a Rigaku Ultima III (Rigaku, Tokyo, Japan) high resolution X-ray diffractometer with Cu K α irradiation. The X-ray generator was operated at 40 kV and 44 mA. The samples were scanned from 2 θ = 10° to 90° using increments of 0.1° and a dwell time at each increment of 20 s. The JADE 7.0 (Materials Data, Inc.) X-ray pattern data processing software was used to determine the crystalline properties, including crystal size, and full width at half-maximum (fwhm).

Electrical Characterization. Nanowires were prepared on p-doped (100) silicon wafers (5–10 Ω cm) with 1 μ m of thermally grown oxide (Silicon Quest International, Inc.). A four-probe gold electrode of 60 nm thickness was evaporated onto a single nanowire using a contact shadow mask. Four contact electrical resistivities were then measured using a SourceMeter (model 2400 Keithley Instruments) in conjunction with a Digital Multimeter (model 2000 Keithley Instruments). The cryogenic high vacuum grease (Apiezon N) was applied to the back of the sample to ensure good thermal contact between the sample and the coldfinger in the cryogenics system. The temperature-dependent nanowire resistivity was measured between ambient and 20 K using a closed-cycle helium refrigerator (model CCS-150 JANIS Research

Company) with a model 8200 compressor (JANIS Research Company). During the experiment, the current was controlled below 1 μ A to avoid any Joule heating. The temperature of the sample stage was controlled by a temperature controller (model 325 Lake Shore Cryotronics) and data acquisition and instrument control were carried out by a computer equipped with Labview (National Instruments).

Electron and Optical Microscopy. Scanning electron microscopy (SEM) measurements were carried out using a Philips model XL-30 FEG SEM operating at 15 keV and a working distance of 10 mm. All samples were sputter-coated with a thin (1–2 nm) gold film onto the glass slides before imaging to prevent charging. Optical microscope images were acquired using a Carl Zeiss Axioskop2 equipped with dark field objectives. Transmission electron microscopy (TEM) was performed on nanowires that were released from the surfaces on which they were synthesized and transferred to TEM grids as free-standing wires. This was accomplished as follows: Linear Au, Pd, or Pt nanowires, deposited onto glass by LPNE at either 5 or 2 μ m interwire pitch, were released from the glass by etching in 2% HF solution for 5 min. A stream of water was then directed onto these surfaces and the nanowires were washed onto carbon-coated copper grids (Ted Pella, Inc.). In the case of bismuth, nanowires were removed from a photoresist coated surface using an acetone rinse and then transferred onto the copper grid. All the grids were dried overnight before TEM measurements. Images and selected-area electron diffraction (SAED) measurements were obtained using a Philips CM20 TEM at an operating voltage of 200 keV. SAED analyses were carried out using an aperture diameter of 100 nm.

AFM Analysis. Intermittent contact mode atomic force microscopy (AFM) imaging was performed in air at ambient pressure and humidity using an AutoProbe CP-Research (Park Scientific Instruments, Sunnyvale, CA; now Veeco Instruments, Santa Barbara, CA) scanning probe microscope. The piezoelectric scanner was calibrated using a 5.0 μ m grating in the xy and z directions using an AFM reference (Pacific Nanotechnology, Santa Clara, CA; model no. P-000-0004-0). The AFM tips were silicon (either Multi75 Metrology Probes, model no. MPP-21100; or Tap300 Metrology Probes, model no. MPP-11200, both Veeco Instruments, Santa Barbara, CA). Topographs were obtained as 256 pixels \times 256 pixels, flattened line by line, and analyzed using the AutoProbe image processing software supplied by the manufacturer.

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